Claims 3 and 7 are rejected under 35 U.S.C. §103(a) as defining subject matter which is allegedly rendered obvious over Applicants' admitted prior art in Figures 1-3 and in view of Kodera, et al. and further in view of the teachings in U.S. Patent No. 5,334,552 to Homma ("Homma"). Finally, Claims 4 and 8 are rejected under 35 U.S.C. §103(a) as defining subject matter which is allegedly rendered obvious over applicants' admitted prior art in Figures 1-3 or in view of Kodera, et al. and further in view of the teachings of U.S. Patent No. 5,429,995 to Nishiyama, et al. ("Nishiyama, et al.").

Applicants have amended the specification, which when considered with the comments hereinbelow, is deemed to place the present case in condition for allowance. Favorable consideration is respectfully requested.

Applicants have amended the specification on Page 2, line 30 to change reference number "14" to "19". The text on Page 2, line 27, refers to a tungsten plug being formed in the viahole 18. Although the text, as originally filed refers to it as reference number 14, a review of the Figure clearly shows that reference number 14 is formed in viahole 13. In addition, it reveals that the reference "19" is formed in viahole 18. Thus, it is clear that this is a typographical error. Thus, there is adequate support in Figure 1 for the amendment.

Similarly, reference numeral 19 in Figure 5 denotes a tungsten plug. The structure to which reference number 19 points is identical in shape and configuration to reference no. 14 in Figure 5 and reference no. 19 in Figure 1. Moreover, reference no. 19 is located in a viahole, just like reference no. 14 in Figure 5 and reference no. 19 in Figure 1. More specifically, reference no. 19 is located in viahole 18 in Figure 1, just as in Figure 5. Moreover, the specification, on Page 13, line 21-24, indicates that the steps from Figure 6 to

Figure 9 are repeated, thereby completing the final structure shown in Figure 5; this provides additional support that, like reference no. 14, reference no. 19 is a tungsten plug. Thus, since reference no. 19 is in Figure 1 and reference no. 14 in Figure 5 are tungsten plugs, reference no. 19 in Figure 5 also denotes a tungsten plug.

Thus, applicants have amended the text on Page 10 to indicate that the steps illustrated in Figure 6 to 9 also form viahole 18 and tungsten plug 19.

Finally, the specification has been amended to reflect that numeral 10 in Figure 7 is fluorine. The discussions of Figure 7 discuss fluorine implantation; the arrows indicate an implantation of an ion. The same markings is used in Figure 12 and it has also been referred to as reference no. 10. The 10 in Figure 7 thus has the same meaning as in Figure 12. Thus, the text supports that reference number 10 represents the implantation of fluorine.

No new matter is added to the application.

A marked up version showing the amendments to the specification is attached. It is entitled "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

In support of its first rejection under 35 U.S.C. §103(a), the Office Action cites the admitted Prior Art and Kodera, et al. The first §103 rejection is divided into two parts. In the first part, the Office Action rejects Claims 1 and 5.

Claim 1 is directed to a semiconductor device having a plurality of wirings juxtaposed with one another and a SiOF insulating film being in contact with the wirings, characterized in that the fluorine concentration of the SiOF insulating film at a wiring gap portion is set to be higher than the fluorine concentration of the SiOF insulating film on the wirings. The subject matter of Claim 5 is directed to a semiconductor device having a plurality of wiring layers each having a plurality of wirings juxtaposed with one another and a

SiOF interlayer insulating film, characterized in that the fluorine concentration of the SiOF interlayer insulating film at a wiring gap portion is set to be higher than the fluorine concentration of the SiOF interlayer insulating film on the wirings.

In each case, the insulating film comprises SiOF both at a wiring gap portion and on the wiring with the fluorine concentration of the SiOF insulating film or at the SiOF interlayer insulating film being higher than the fluorine concentration of the SiOF insulating film on the wirings or the SiOF interlayer insulating film on the wirings, respectively. Neither the admitted prior art nor Kodera, et al. disclose or suggest this feature.

According to the Office Action, with respect to the subject matter of Claims 1 and 5, the Office Action alleges that the admitted Prior Art discloses the following:

(a) a semiconductor device having a plurality of wirings juxtaposed with one another, and

(b) a SiOF insulating film being in contact with the wirings.

The Office Action admits that the Applicants' admitted prior art fails to disclose the following:

(a) the fluorine concentration of the SiOF insulating film at a wiring gap portion is set higher than the fluorine concentration of the SiOF insulating film on the wiring.

Kodera, et al. fails to overcome the deficiency. Kodera, et al. disclose a semiconductor device having a first through fourth wiring layers formed on the surface of a silicon substrate and a silicon oxide layer containing fluorine deposited over the wiring layers and the silicon substrate and then another silicon oxide layer containing no fluorine is deposited over the silicon oxide layer containing fluorine. Subsequently, the silicon oxide layer containing no fluorine is flattened by polishing at for a predetermined length of time,

when the silicon oxide layer containing fluorine serves as a stopper; according to Kodera, et al. this is because the polishing rate of the silicon oxide layer containing fluorine is lower than that of the silicon oxide layer containing no fluorine.

The Office Action alleges that Kodera, et al. disclose a semiconductor device wherein the fluorine concentration of SiOF (26) at the wiring gap is higher than the concentration of the insulating film (27) on the wirings. It further alleges that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of applicants admitted prior art to include a higher fluorine concentration of SiOF at the wiring gap than at the concentration of the insulating film or the wiring.

Contrary to the allegations in the Office Action, Kodera, et al. do not overcome the deficiency of the prior art. Applicants agree with the Office Action that layer (26) contains SiOF with greater than 1% by weight fluorine. According to Kodera, et al., layer 26 is formed by plasma CVD, wherein a TEOS gas to which NF_3 is added is used as a material gas. However, the silicon oxide layer (27) is not comprised of SiOF. As specifically stated in Column 3, lines 39-46, silicon oxide layer 27 contains no fluorine (not more than 0.1% by weight of fluorine). It is formed over silicon oxide layer 26 by plasma CVD, wherein a TEOS gas to which NF_3 is not added as a material gas. Thus, silicon oxide layer 27 does not contain any SiOF; it contains SiO_2 and/or some fluorine impurities. Thus, contrary to the allegations in the Office Action, Kodera, et al. do not disclose a semiconductor device wherein the fluorine concentration of the SiOF insulating film at a wiring gap portion is higher than the fluorine concentration of the SiOF insulating film on the wiring.

On the contrary, the combination suggests a semiconductor device wherein the insulating film on the wiring is SiOF or SiO_2, i.e., they are interchangeable. But, the combination does not teach, disclose or suggest the semiconductor device wherein the fluorine concentration of SiOF insulating film or SiOF interlayer insulating film at a wiring gap portion is higher than the fluorine concentration of the SiOF insulating film on the wirings or the SiOF interlayer insulating film on the wirings, respectively.

Furthermore, there are advantages when the fluorine concentration of the SiOF insulating film or SiOF interlayer insulating film at the wiring gap portion is higher than the fluorine concentration of the SiOF insulating film on the wirings or the SiOF interlayer insulating film on the wirings, respectively. Attention is directed to Page 11, line 1 to Page 12, line 5 and Figure 10 referred to therein of the present application. The text describes the preparation of a representative semiconductor device and comparison with a semiconductor device in which the interlayer insulating film and a wiring gap portion both were comprised of SiOF and the fluorine concentration was uniform in the interlayer insulating film As shown in Figure 10, the thickness of the wiring made of aluminum film together with the barrier metal layer film in all of the samples is 0.6 um. Moreover, the line width of the wiring/special interval of the wiring L/S in all of the samples is 0.3um/0.3um. As shown by Figure 10 and discussed in the text of the specification, when the fluorine concentration is high, such as 7 atom % for both the prior art and the present invention, the amount of exfoliation in the representative semiconductor of the present invention is zero, as compared to about 10 per wafer in the prior art reference. Thus, where fluorine concentration is high, the semiconductor of the present invention has significantly less exfoliation. In fact, the exfoliation of the semiconductor of the present invention is zero. Further, if the fluorine

concentration is low, e.g. 4 atom%, for both the prior art and in the present invention, the wire capacitance is reduced by about 7%. The 7% reduction in capacitance of the present invention relative to the prior art semiconductor device is quite significant and marks an unexpected decrease of capacitance. It is to be noted that the same advantages described on Page 11 with respect to Figure 10 is also obtained with the second embodiment of the present invnetion.

It should also be noted that the above-mentioned advantages in capacitance is not present on a device wherein the insulating film on the wiring comprises SiO_2 with less than 1% by weight is fluorine. In this case, the capacitance reduction is less than 1%. However, the present invention exhibits a reduced specific dielectric content with respect to the film interposed between the neighboring wiring layers, relative to a device in which the interlayer insulating film at the wiring gap is SiOF and the interlayer is SiO_2 rather than SiOF.

Thus, this information is compelling - - the present invention represents a patentable departure over the prior art.

Thus, for reasons given, the rejection of Claims 1 and 5 under 35 U.S.C. §103(a) is obviated; withdrawal thereof is respectfully requested.

Claims 2 and 6 are dependent upon Claims 1 and 5, respectively. The subject matter in Claim 2 is directed to a semiconductor device described in Claim 1 which additionally has a SiOF insulating film at the wiring gap portion comprising a first SiOF film and a second SiOF film formed on the first SiOF film, the SiOF insulating film on the wiring comprising the second SiOF film and the fluorine concentration of the first SiOF film being higher than the fluorine concentration of the second SiOF film. In addition, the subject matter in Claim 6 is directed to a semiconductor device described in Claim 5, wherein the SiOF

interlayer insulating film at a wiring gap portion comprises a first SiOF film and a second SiOF film formed on the first SiOF film, the SiOF interlayer insulating film on the wirings comprises the second SiOF film, and the fluorine concentration of the first SiOF film is higher than the fluorine concentration of the second SiOF film.

With respect to the rejection of Claims 2 and 6 under 35 U.S.C. §103(a), the Office Action alleges that the applicants' admitted prior art disclose a SiOF insulating film at a wiring gap portion comprising a first SiOF film and a second SiOF film formed on the first SiOF, with the SiOF insulating film on the wiring comprising the second SiOF film. However, the Office Action admits that applicants' admitted prior art does not disclose that the fluorine concentration of the first SiOF film is higher that the fluorine concentration of the second SiOF film.

Contrary to the allegations of the Office Action, Kodera, et al. do not overcome the deficiencies. As indicated hereinabove, the insulating film on the wiring (27) in Kodera, et al. is not comprised of SiOF, but rather is SiO_2, containing at most 0.1% fluorine impurities. Applicants reiterate the comments hereinabove and incorporate the same by reference. The SiOF in layer (26) is comprised of SiOF, since it is formed by plasma CVD in which a TEOS gas to which NF_3 is added is used as a material, layer (27) in Kodera, et al. however, although is formed plasma CVD, it is not formed by the use of a TEOS gas to which NF_3 gas is added as a material gas. Thus layer 27 is not comprised of SiOF. Thus, Kodera, et al. do not disclose a semiconductor device where the fluorine concentration of the first SiOF film is higher than the fluorine concentration of the second film comprised of SiOF, as alleged by the Office Action. Thus, the combination of Kodera, et al. with applicants admitted prior art fails to teach, disclose or suggest a semiconductor device wherein the fluorine

concentration of the SiOF insulating film or a SiOF interlayer insulating film at a wiring gap portion comprises a first SiOF film and a second SiOF film formed on the first SiOF, wherein the fluorine concentration of the first SiOF film is higher than the fluorine concentration of the second SiOF film. Further the combination does not teach, disclose or suggest that the SiOF insulating film on the wirings or SiOF interlayer insulating film on the wirings comprises the second SiOF film, i.e., the same film as the second SiOF film formed on the first SiOF film and that the fluorine concentration of the first SiOF film is higher than the fluorine concentration of the second SiOF film.

Moreover, the arguments presented hereinabove with respect to the non-obviousness of Clams 1 and 5 are reiterated and are incorporated herein by reference. Further, since Claims 1 and 5 are patentable over the prior art and since Claims 2 and 6 respectively depend from Claims 1 and 5, the subject matter of Claims 2 and 6 are also patentable over the prior art.

Therefore, for the reasons given hereinabove, the rejection of Claims 2 and 6 under 35 U.S.C. §103 is obviated, withdrawal thereof is respectfully requested.

In support of the rejection of Claims 3 and 7 under 35 U.S.C. §103(a) the Office Action cites applicants admitted prior art, Figures 1-3 in view f Kodera, et al. and further in view of U.S. patent No. 5,334,552 to Homma ("Homma"). According to the Office Action. Homma is being cited for its alleged teaching of a semiconductor device wherein the thickness of the SiOF film is 1/3 to 1/1 times the thickness of the wirings.

Applicants disagree that Homma in Column 2, lines 42-54 discloses a semiconductor device wherein the SiOF is 1/3 to 1/1 times the thickness of the wirings. In Column 2, Homma disclose the fluorine containing silicon oxide film may reach 3.5 um. But,

the reference in Column 2, lines 43-54 does not provide the thickness of the wirings of the semiconductor device. However, assuming pro arguendo, that Homma does teach a semiconductor device wherein the thickness of the SiOF film is 1/3 to 1/1 times the thickness of the wirings, it does not overcome the deficiencies of Kodera, et al. discussed hereinabove in the arguments traversing the '103 rejection. More specifically, it does not teach, disclose or suggest a semiconductor device wherein the fluorine concentration of the SiOF insulating film at a wiring gap portion or the SiOF interlayer insulating film at the wiring gap portion is set higher than the fluorine concentration of the SiOF insulating film on the wirings or the fluorine concentration of the SiOF interlayer insulating film on the wirings, respectively, as recited in Claims 3 and 7. Moreover, it does not teach, disclose or suggest that the SiOF insulating film or the SiOF interlayer insulating film at a wiring gap portion comprises a first SiOF film and a second SiOF film formed on the first SiOF film and the SiOF insulating film or SiOF interlayer insulating film, respectively, also comprise the second SiOF film, wherein the fluorine concentration of the first SiOF film is higher than the fluorine concentration of the second SiOF film. Thus, the arguments traversing the first '103 rejection discussed hereinabove is reiterated and incorporated herein by reference. Since the combination of the references do not teach, disclose or suggest this subject matter, as described hereinabove and since the combination does not teach, disclose or suggest the unexpected results, described herein and shown by the data, the rejection of Claims 3 and 7 under 35 U.S.C. §103 is overcome; withdrawal thereof is respectfully requested.

Pursuant to the rejection of Claims 4 and 8 under 35 U.S.C. §103(a), the Office Action cites applicants admitted prior art in Figures 1-3 in view of Kodera, et al. and further in view of Nishiyama, et al.

Nishiyama, et al. is being cited for its teaching that a silicon oxide film can be prepared having a fluorine concentration of 3 to 8%. However, Nishiyama, et al. fail to disclose a semiconductor device wherein the fluorine concentration of the SiOF insulating film at a wiring gap portion is higher than the fluorine concentration of the SiOF insulating film on the wirings. Thus, it does not overcome the deficiencies of Kodera, et al. which are described in the first '103 rejection, the contents of which are incorporated herein by reference.

Moreover, although Nishiyama, et al. teaches that a SiO_2 film having a fluorine concentration ranging form 3 to 8% can exist, even if combined with the other references and even if the combination of Kodera, et al. with applicants admitted prior art suggest what is alleged in the Office Action, a position which applicants do not agree with, the combination does not teach, disclose or suggest that the fluorine in the first SiOF film is 5 atom % or more and the fluorine concentration of the second SiOF film is less than 5 atom %. Even if it were argued that Kodera, et al. suggest that the SiOF insulating film at a wiring gap portion is higher than that fluorine concentration of the SiOF insulating film on the wiring, which is alleged by the Office Action - - a position with which applicants disagree-- there is no suggestion in the combination as to the amounts of fluorine present in the insulating film at the wiring gap or in the insulating film at the wirings. There is no teaching that would suggest that the former would have a concentration of 5 atom % or greater and the latter having a concentration of 5 atom % or less.

Thus, for the reasons given herein, the rejection of Claims 4 and 6 under 35 U.S.C. §103(a) is obviated; withdrawal thereof is respectfully requested.

The Office Action alleges that Claim 1 is a duplicate of Claim 5. Applicants disagree. Claim 1 is directed to the semiconductor device having one wiring layer containing a plurality of wirings, while Claim 5 is directed to the semiconductor device having a plurality of wiring layers, each containing a plurality of wirings. This distinction is further emphasized by the terms used in Claims 1 and 5. More specifically, the term "SiOF insulating film" is used in Claim 1 while the term "SiOF interlayer insulating film" is used in Claim 5. Thus, the use of different terms clearly indicate that the scope of these claims is not identical. The "SiOF interlayer insulating film" comprises a SiOF insulating film in one layer of the wiring structure, but the "SiOF interlayer insulating film" comprises a plurality of wiring layers. Thus, Claim 5 does not claim the same subject of Claim 1.

Thus, in view of the Amendments to the specification and the Remarks herein, ti is respectfully submitted that the present case is in condition for allowance; which action is earnestly solicited.

Respectfully submitted,

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MJC:lf

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification has been amended follows:

Please replace the paragraph that begins on Page 2, line 28 with the following:

Subsequently, as shown in Fig. 1, a third interlayer insulating film 17 having a viahole 18 is formed, a tungsten plug [14] 19 is formed in the viahole 18, and a barrier metal layer 5C, an aluminum layer 6C and a titanium nitride layer 7C are successively formed. Thereafter, a desired pattern is left to form the third layer wiring 20. Then, a cover film 21 is formed, thereby completing the final structure shown in Fig. 1.

Please replace the paragraph that begins on Page 9, line 4 with the following:

Subsequently, as shown in Fig. 7, SiOF film 9 is subjected to an anisotropic etching by reactive ion etching to remove SiOF on the upper surface of the first layer wiring 8. At this time, SiOF film 11 remains having about a half of the thickness of the first layerwiring 8 at the center in the gap portion of the first layer wiring. In this state, fluorine (10) is ion-implanted, for example under the following conditions: an acceleration energy of 10 keV to 100 keV and a dose amount of 5×10^{14} cm^{-2} to 3×10^{15} cm^{-2}. SiOF is removed by the etching also in the gap portion of the first layer wiring 8, and thus the thickness of the SiOF film 11 at the center in the gap portion of the first layer wiring is equal to about a half of the thickness of the first layer wiring 8. In consideration of reduction in wiring capacitance, it is preferable that the thickness of the SiOF film 11 at the center of the wiring gap portion is within the range of 1/3 to 1/1 times of the thickness of the wiring 8, and it is more preferable that the wiring gap portion is filled with thicker SiOF film 11 or perfectly filled SiOF film 11.

Please replace the paragraph that begins on Page 10, line 21 with the following:

Subsequently, the steps from Fig. 6 to Fig. 9 are repeated once again to form a viahole 18, tungsten plug 19, the third layer wiring 20, and a cover film 21 of SiON or the like is finally formed, thereby completing the final structure shown in Fig. 5.